Date: ____3/5/2021_____

EIC Detector R&D Progress Report

Project ID: eRD24__
Project Name: A Proposal for Silicon Detectors with high Position and Timing Resolution as Roman Pots at EIC
Period Reported: from 7/2020 to 2/2021
Project Leader: _____
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Abstract

Roman Pots are an integral part of the detector system of an EIC and essential for the success of its physics program. Roman Pots will provide a critical contribution to the study of exclusive production processes in ep collisions, i.e. deeply virtual Compton scattering as well as tagging protons from deuteron breakup in eA interactions, among others. This proposal aims at setting the performance requirements for a Roman Pot detector at EIC, focusing on spatial granularity, timing resolution and acceptance. In addition, an innovative silicon-based technology, called Low Gain Avalanche Diode (LGAD), will be studied as it has the potential to combine in a single sensor fine spatial resolution and precise timing. More specifically, the AC-coupled version of LGADs (AC-LGADs) will be studied and prototypes fabricated at BNL to establish spatial and timing performance as well as the minimal possible inactive area that is critical for placing such sensors as close as possible to the beam. Given the need of fast-timing at EIC and the growing interests in LGAD technology to meet those needs, the scope of this proposal is expanded to include the study for the application of such technology in other detector designs for EIC, i.e. a pre-shower calorimeter. Additionally, we intend to collaborate with colleagues who have proposed such technologies for tracking and TOF. In response to recommendations from the committee, we have expanded the scope of the proposal and strengthened the team of co-investigators to include the development of an architecture for the readout electronics and experts in readout electronics and ASIC design.

Past

What was planned for this period?

The work planned for this period was structured in three main tiers:

1) Studies of physics performance and detector specifications (Roman Pots and Preshower):
    a) Studies of beam+gas background and occupancies
    b) Design of an edgeless sensor, and the impact to low-p_T acceptance
    c) Layout of "strawman" sensor layout
2) Detector R&D (slim-edge and pixelated AC-LGADs)
    a) Fabrication of zigzag strips and testing
    b) Design a double-metal technique for the definition of complex 2D metal patterns
    c) Investigate the trench termination as a slim-edge option
    d) Start new fabrication of AC-LGADs with larger area and different electrode designs
3) Start the design of a read-out architecture
    a) Study a readout ASIC architecture with 500 micron pitch, starting from the ATLAS ALTIROC chip, and identify the missing blocks to be designed.
    b) Assemble an ALTIROC prototype for ATLAS with an AC-LGAD to study compatibility and performance of the Very Front End (preamplifier, discriminator + TDCs).
    c) Study alternative low-power ASIC technologies.

What was achieved?

Here follows a status report of the work carried out in this period.

Simulation studies have been carried out to estimate the beam+gas background impact on the Roman Pot sensors. Before any studies were carried out, some simple calculations were performed to understand the occupancies expected on the Roman Pots sensors, based on the machine luminosity. In Chapter 3 of the EIC Conceptual Design Report (https://www.bnl.gov/ec/files/EIC_CDR_Final.pdf), Tables 3.3 - 3.5 summarize the machine parameters for various configurations. Using the maximum design luminosity of $10^{34} cm^{-2} s^{-1}$ and an e+p cross section (for 10x275 GeV collisions) of $\sim 50 \mu b$, we get a DIS collision rate of 500kHz. For any DIS event, it is only possible for 1 proton to be produced in the Roman Pots detector acceptance. Given an active area of 25cm x 10cm for the detector, and 0.05cm square pixels, this leads to an occupancy of 5 hits/pixel/second.

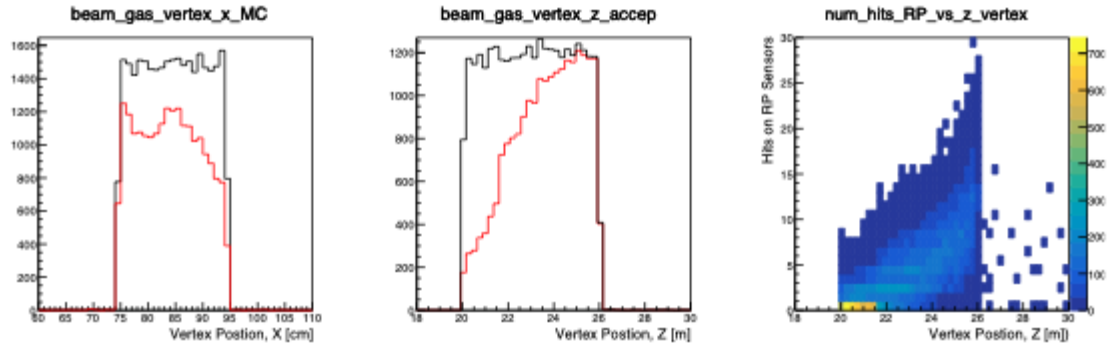

Figure 1: The x and z vertex positions for the beam+gas collisions (left, middle) in black, and the events for which particles were incident on the Roman Pots sensor planes in red. The right plot shows the number of particles incident on the Roman Pots from a beam+gas event as a function of the z-vertex position.

For background rates, assuming a vacuum of 10^{-9} mbar, a 1.0 A proton beam current (as seen in Table 3.3 for the 10x275 GeV configuration), and a beam+gas cross section of ~ 60mb (the cross section for p+H2 collisions in the pipe). H2 is the dominant gas in the ultra-pure vacuum environment in the beam pipe near the Roman Pots subsystem. The background rate is then only dependent on the effective length of the beam pipe that can possibly produce a beam background event. Figure 1 shows the (x,y,z) vertex positions for fixed target PYTHIA p+p events ranging from z = 20m (still partially inside the B1apf dipole) to z = 26m (just in front of the first Roman Pots plane). The PYTHIA p+p events serve as stand-in for p+H2 collisions, with the cross section accordingly scaled in the estimation of the background rates. The figure shows that the probability for produced particles to be incident on the Roman Pots detector to drastically decrease as the beam+vertex moves further out of the drift and into the lattice. This is because the produced beam+gas background particles are at much lower momentum than the beam, and are therefore strongly bent by the dipole magnets out of the beamline before reaching the Roman Pots. In calculating the beam+gas background rate, assuming an effective length of beam pipe for a significant probability of a collision of 500 cm is a reasonable estimate. Using these numbers, the effective beam+gas background rate is ~5 kHz, two orders of magnitude below the DIS collision rate. Additionally, these events will take place significantly out of time with the collisions at the IP, allowing the fast timing resolution of the Roman Pots to easily reject these background particles.

As a result of simulation efforts for the EIC Yellow Report, further studies of different collisions systems were undertaken. In the case of e+He-3 collisions, the needed active area for the Roman Pots sensors were reinforced. In e+He-3 collision, the spectator protons in an incoherent nuclear breakup event have ⅔ the rigidity of the He-3 beam. Something similar has also been observed with e+d events where the breakup protons have ½ the beam rigidity, but the effect on the protons in the two cases is different in terms of detector acceptance. In the e+d case, the protons are almost entirely bent out of the beam pipe after the B1apf dipole, requiring the Off-Momentum Detector system for tagging. However, in the e+He-3 case, the protons are bent less than in the e+d case, and

they therefore primarily end up in one side of the Roman Pot sensor plane, as shown in Fig. 2. This further reinforces the need for a large active area for the Roman Pots sensor.

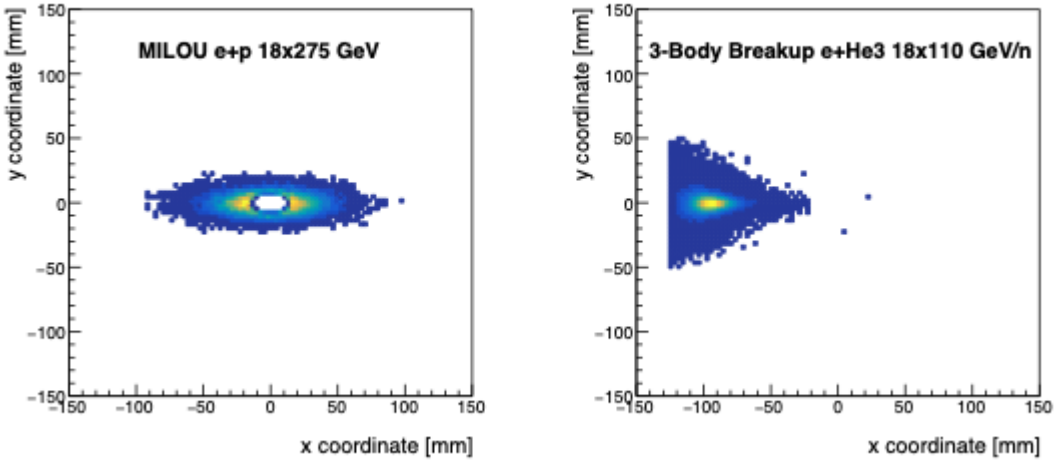

Figure 2: The incident proton's hits on the Roman Pots sensor plane for e+p DVCS events (left) and e+He3 3-body breakup events (right). Both plots show the coordinates local to the sensor plane, with the sensor plane having a size of (x,y) = (25 cm, 10 cm) in the simulation.

A layout of the Roman Pots detector was developed, referred to in the following as Strawman, and is used for the development of the sensors, readout electronics and mechanical system as well as for cost estimation. Figure 3 shows the Strawman design. It includes 2 stations, about 2 m apart, of 2 layers each. Each layer comprises a top and bottom part with a C-shape to provide full geometrical coverage. Figure 4 also shows the geometrical dimensions of the main elements.

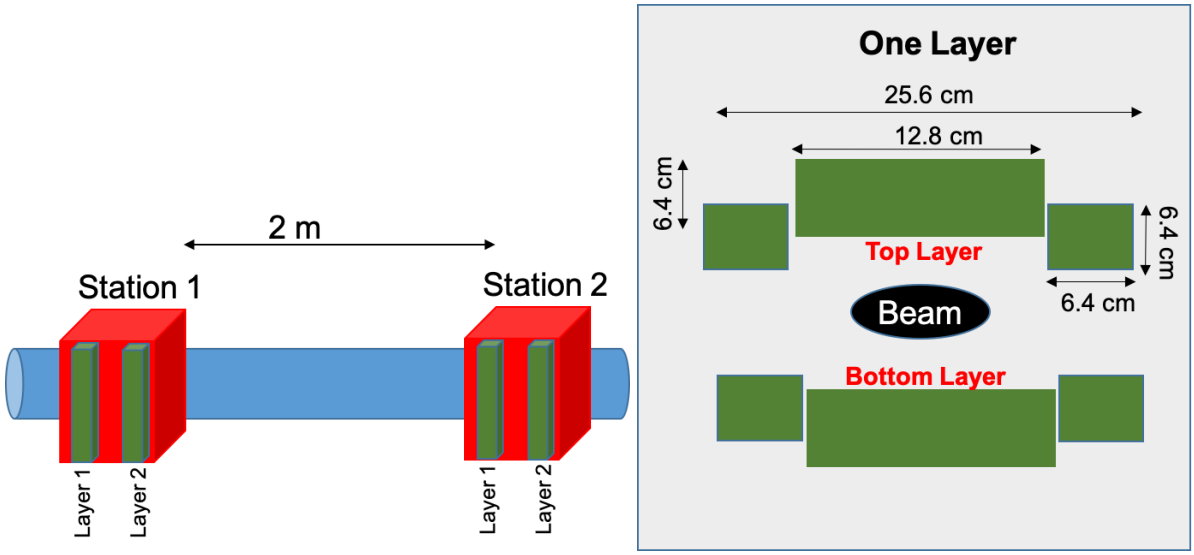

Figure 3: Strawman layout of the Roman Pots detector (left), comprising 2 stations with two layers each, and layout of one layer (right) that comprises a top and a bottom part.

In collaboration with ASIC designers, we developed a design of the modules, each comprising a silicon sensor of 3.2 x 3.2 cm^2 and 4 ASICs of 1.6 x 1.8 cm^2, as sketched in Fig. 4. The ASICs will include 32 x 32 channels of 500 micron pitch that match the sensor pixel pitch of 500 x 500 μm^2. The Strawman design includes a total silicon sensor area of 1,311 cm^2 divided into 128 modules (32 per layer), and 512 ASICs for a total number of 524,288 channels.

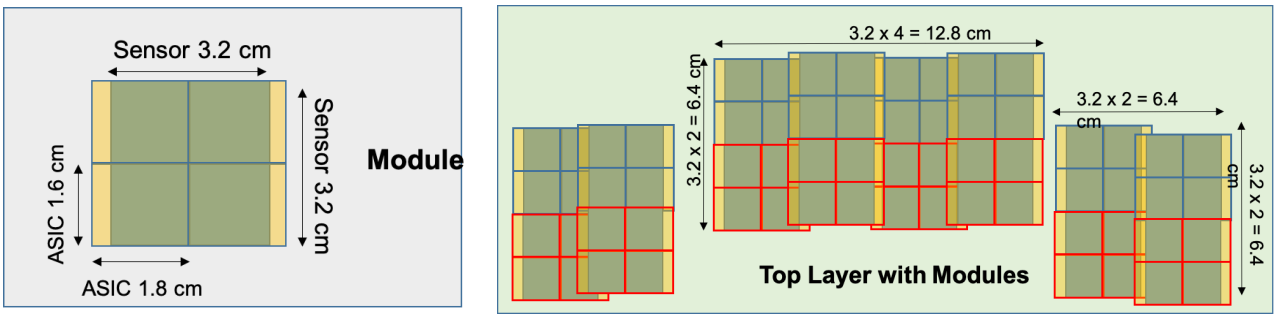

Figure 4: Strawman layout of a module (left) comprising one sensor and 4 ASICs, and the top part of a layer within a station (right) that comprises 16 modules arranged in a C-chape. The bottom part of the layer will have the same layout as the top part.

1. *Detector R&D*

A small batch featuring zig-zag devices has been carried out at BNL, in addition to a batch with a modified layout and process flow. The substrates are of the same kind as those used in the previous fabrications of LGADs (4" diameter, 50 µm thick p-type epitaxial layer). The wafer includes many devices, with areas up to 1.4 cm x 1.4 cm, with a modified termination structure, see Figure 5 below. A slim termination has also been used in a few test devices. The addition of a trench termination has been deemed unnecessary. Together with the new mask set, also the process has been modified, as to correct flaws from the preceding productions and address points that have arisen from the intensive tests of former LGADs. In particular, the process features one less lithography and a deeper p-type gan layer. The new process however required re-calibration of the gain layer dose. In this first production the dose was too high, resulting in a breakdown voltage slightly less than the depletion voltage, which for these wafers is relatively high. However, other wafers are now in production that will address this point by lowering the dose of the gain layer. When we receive inputs from the beam test results, we will design a new metal, to be used in two other wafers that are on hold.

Several tests of AC-LGADs were carried out at BNL and at test-beams, and simulations were performed to better understand the signal sharing properties in AC-LGADs and optimise the sensor design.

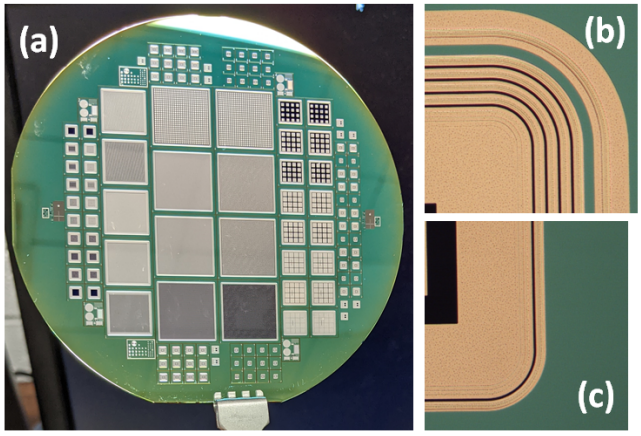

Figure 5: (a) picture of a 4" silicon wafer with the new layout. (b) corner of a device, showing the new termination, (c) slim termination featured in a subset of devices.

The time resolution of an AC-LGAD was measured with a new setup (beta-scope) put in place at BNL that uses beta particles from a radioactive 90Sr source to detect coincidence signals between the DUT and a reference device. For this test a Hamamatsu LGAD sensor of 35 μm thickness, gain of 55, and a known time resolution of 28 ps was used as reference, while the DUT was a pixel AC-LGAD sensor of 50 um active thickness, gain of about 20, a pitch of 220 um and 20 um gap between pixel metals that was operated at a bias voltage of -210 V and read out via a fast-time amplifier board developed by UCSC. The results yielded a time resolution of 46 ps, which compares well with results obtained at the FNAL test-beam (as reported in the previous period), and with LGADs of similar gain. Figure 6 shows the time resolution measured as a function of the Charged Fraction discriminator (CFD) thresholds set on the reference ("Trigger") sensor and on the DUT. This results confirms that the optimal CDF operating points are for 20-30% for the DUT and 50-60% for the "Trigger" sensor, as found for conventional LGADs. In a more recent test-beam at FNAL (March 2021) preliminary results show that at higher bias voltage the same sensor can reach 34 ps time resolution.

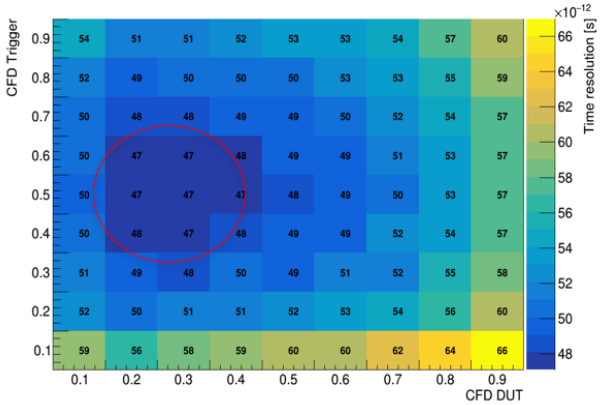

Figure 6: Time resolution of a BNL's AC-LGAD pixel sensor with 220 um pitch as a function of CFD thresholds for the Reference ("Trigger") and the DUT sensors.

Basic performance of the first zig-zag AC-LGAD was tested at BNL for the first time using beta particles. The device included three structures fabricated with different pitches (500 µm, 200 µm, 100 µm), with an inter-strip gap of 10 µm, and strip length of 800 µm, as a bias voltage at -400 V, see Figure 7 (left). The tests included measurements of signal shapes, amplitudes and correlations of signals in three adjacent channels, see Figure 7 (right), compared to those of a strip sensor. The results were positive, however for accurate study of space resolution, similar zig-zag sensors were sent to test-beams at FNAL, as detailed below, for a precise determination of the position of the incident particle.

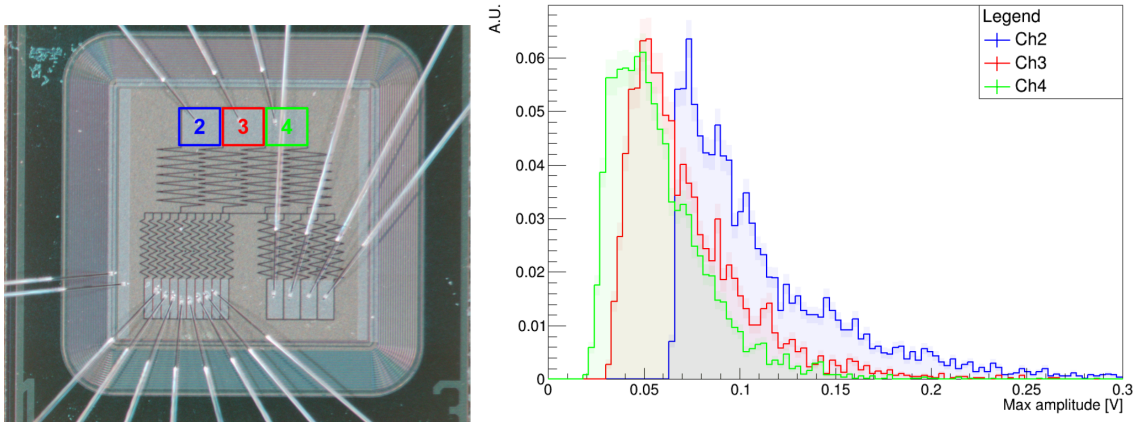

Figure 7: photo of an AC-LGAD device with three zig-zag structures with different pitches (left), and signal amplitudes (right) from beta particles as measured in three channels (Ch2,3,4) corresponding to the top sensor in the left-hand-side photo.

Measurements of charge collection were performed on an AC-LGAD with an IR laser, using the Transient Current Technique (TCT) to test the uniformity of the signal collection on the sensor surface and signal sharing properties. More tests are planned for the next period on more structures. Figure 8 shows the map of charge collected by a strip (2nd strip from the left-hand side in the photo) when the laser hit position is scanned over the sensor surface. The plot shows the effect of reduction in signal as the laser hits the sensors farther away from the readout strip along the x-direction (signal sharing effect).

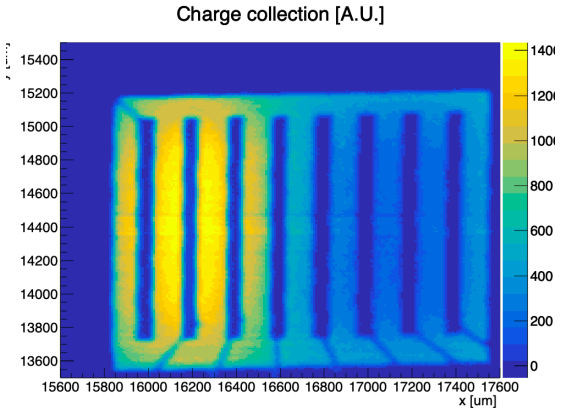

Figure 8: Collected charge (in arbitrary units) as a function of the IR hit position on the x-y plane of the sensor, with a 10 µm spatial granularity. The signal is seen only in gaps between strips, as the strip electrodes are metalised.

Several sensors fabricated at BNL were sent to 2 different test-beams at FNAL to be tested with a 120 GeV proton beam. These sensors include some LGADs used as references, AC-LGADs with strip, pixel and zig-zag metal geometries. The AC-LGADs were fabricated with different pitches and metal shapes (i.e. squares and hexagonal) to assess the effect of signal sharing and its impact on spatial resolution. Figure 9 shows a sample of AC-LGADs tested at the FNAL test-beams. The goals of these two test-beams are to confirm the expectation for time resolution, and study in greater detail the space resolution as a function of pitch variation and electrode geometry.

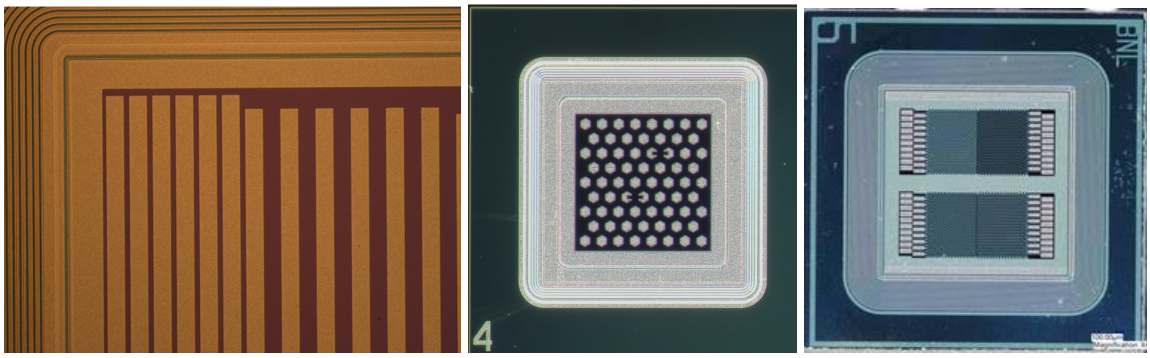

Figure 9: AC-LGAD sensors with varied metal designs: variable strip pitch (left), hexagonal pixels (middle), four zig-zag structures with different designs (right).

One test-beam took place in February, and the other in February-March, in collaboration with colleagues from ANL and FNAL. While preliminary results are positive, indicating a time resolution of 34 ps and a space resolution better than 15 μm for a strip detector with 100 μm pitch, a more thorough data analysis is on-going.

TCAD simulations were conducted to study signal dependence on pixel geometry and layer designs, e.g. pixel width, oxide thickness, doping (i.e. resistivity) of resistive layer, with the goal to gain insight on the signal sharing effect between adjacent pixels and optimise it to improve spatial resolution. Studies included simulations of amplitudes vs inter-pixel gap size, at fixed pixel size, for the hit and adjacent pixels as a function of several implantation doses of the resistive (n+) sheet. For the pixel directly hit by the particle, it was found that the signal fraction in the hit pixel increases as resistivity increases, while its signal fraction decreases as pixel gap increases. For pixels adjacent to the hit one, a larger signal fraction is seen as the resistivity decreases. As the resistivity increases, the amplitude ratio to substrate increases for wider gaps (the signal sharing is between hit and adjacent pixel only), while as the resistivity decreases the amplitude ratio to substrate decreases for wider gaps (the sharing is among several neighboring pixels). The results of the simulations will be quantitatively compared to results from test-beams in the following period.

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The UCSC SCIPP group focused their sensor R&D activities on AC-LGAD produced at FBK with support from INFN Torino. The emphasis is to understand the dependence of the overall performance parameters i.e. temporal and spatial resolution on detector

parameters which are varied by the manufacturer. This includes the geometrical layout of the ac-coupled readout pads (pitch and size), the thickness of the coupling oxide, the doping profile of the n^{++} layer including the resulting sheet resistance, the external termination resistor of the n^{++} layer to ground, the doping profile of the p^{+} gain layer. Two important detector parameters could not be directly investigated, namely the bulk thickness and the infusion of carbon into the gain layer to improve the radiation resistance. We expect thinner sensors including carbon to be available within this year. All FBK sensors had a thickness of nominal 55 µm and a gain of about 10. A large variation of pixel pitch and pad metal size were investigated. In anticipation of large-scale use at the EIC, we concentrated on the sensors with pitch in excess of 100 µm in order to satisfy a realistic power requirement (comparable to the power density of the HGTD electronics) and pad size above 100 µm to permit bump bonding and reduce the capacitance.

In the following we show results from detailed investigations performed using an IR laser which is focused to ~20 µm spot size. In order to understand the signal formation both under the metal pads and in the area not covered by the metal, we removed the metal on the back side on some of the sensors and performed scans both from the front and the back of the sensors. Fig. 10 shows a 2D plot of the pulse height close to a pad in a 500-200 (pitch = 500 µm, Pad Size = 200 µm) sensor and the pulse shapes on the locations indicated by the red dots from scans from the front (on the left) and from the back. There are several important conclusions: with the exception of the pulse height the pulse shapes are to first order independent of the location, the signal height underneath the metal pad is constant, underneath the next neighbor of the order 10% and under the next to next neighbor pad less than 2%, respectively. Since the signal height below the metal provides essentially no information on the location of the laser spot, the size of the metal in the pads of the eIC detectors need to be minimized.

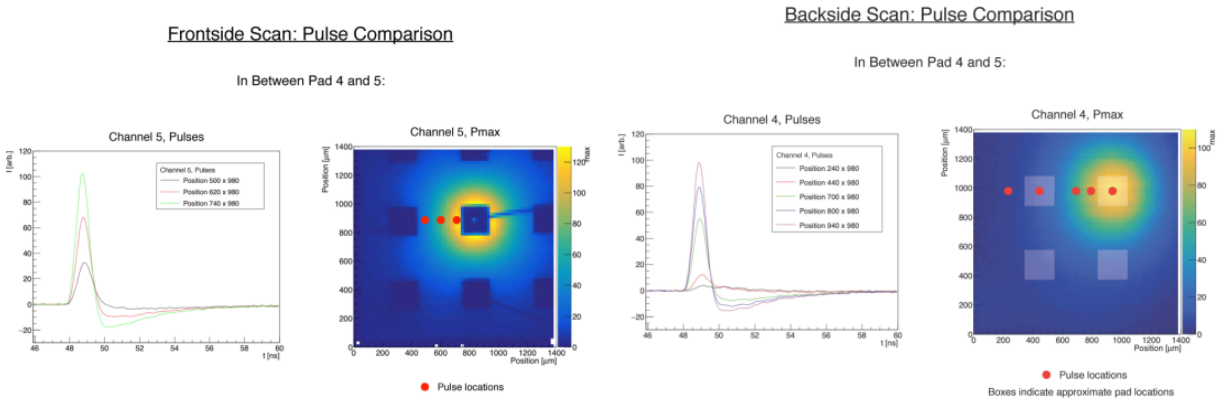

Figure 10: Pulse heights and corresponding pulse shapes at distinct locations for IR scan performed from the front (left) and the back (right) on a 500-200 µm pitch sensor.

The required distance between pads was studied with the sensors 500-490, (pixel size 500 µm x 500 µm and pad size 490 µm x 490 µm). They have an inter-pad distance of 20 µm. A laser scan across the back of the sensors is shown in Fig 11. Both the 2D plot and the pulse height profile indicate a constant signal in the next neighbor caused by capacitative

pick-up, which is also shown by the bipolar pulse shape under the next neighbor pad in Fig. 11. This pick-up will reduce the position resolution between pads. A scan across a sensor with inter-pad distance of 50 µm does not show this capacitative pick-up and so 50 µm is judged to be a safe inter-pad distance.

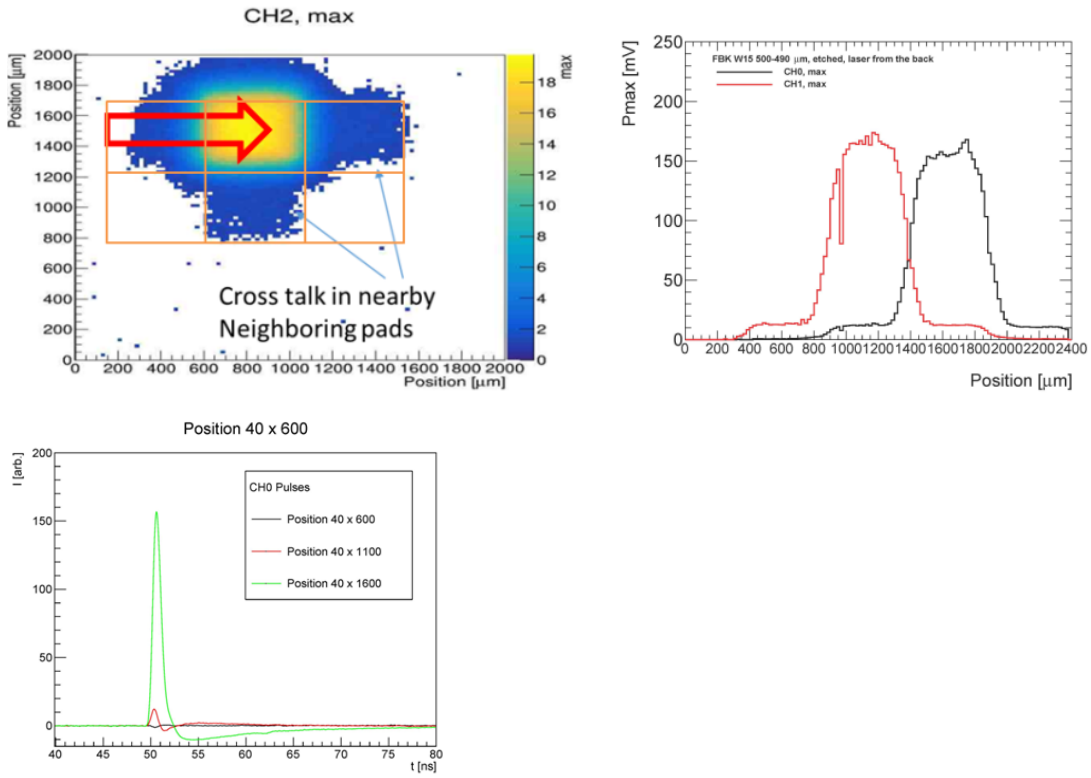

Figure 11: Laser scan across the back of the sensor 500-490, showing pick-up in the next neighbor in the 2D plot (top-left), the pulse height profile (top-right) and the pulse shape (bottom).

The effect of the doping of the n^{++} layer was investigated with laser scans on three sensors with the n^{++} doping density increasing by a factor 2. The doping density of W8 is about 1/10 of what is usually used in LGAD, and the one of W3 is a factor 2 lower and the one of W13 is a factor 2 higher. As Fig. 12 shows, there are small but visible differences in height and rise time between the sensors. W3 with the lowest n^{++} dose, exhibits a reduced pulse height and increased rise time close to the adjacent pad when compared with W8 and W13 (Fig. 3 right). The profiles in Fig. 13 show a reduced pulse height (Fig. 13 left) and increased jitter (Fig 13 right) close to the neighboring pad for W3 having the lowest n^{++} dose.

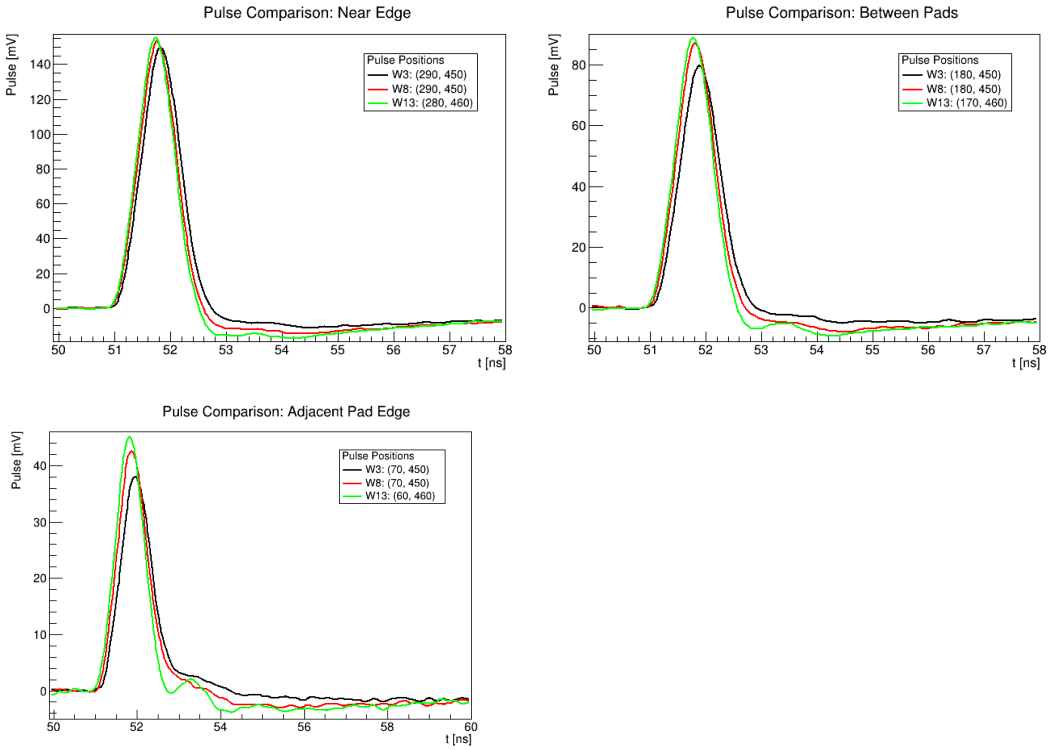

Figure 12: Pulse shapes of the three sensors near the edge of the pad with readout (ltop-eft), in the middle between pads (top-right) and next to the adjacent pad (bottom).

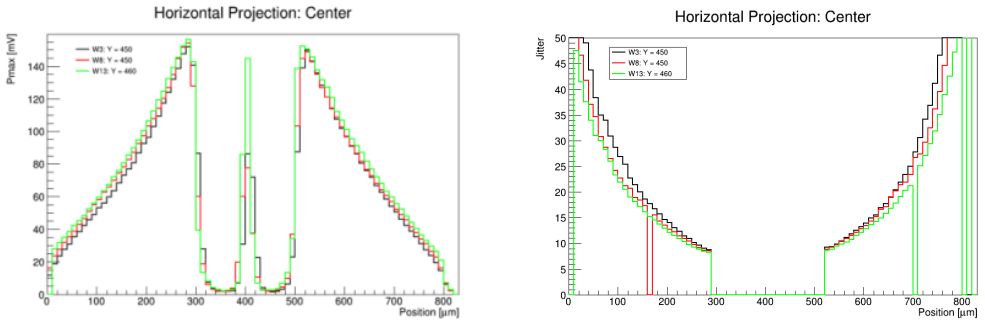

Figure 13: Pulse height (left) and jitter (right) for the three sensors with different N^{++} dose, indicating the lower pulse height and increased jitter close to the adjacent pad for W3 with the lowest dose.

The effect of the termination of the n^{++} layer has been investigated by front laser scans on a detector terminated either directly to ground or via a 1 MΩ resistor. Fig. 14 shows the 2D plot of the pulse height (left), and the resulting profiles of pulse height (center) and of jitter (right). The scans for the two different termination resistances are indistinguishable, although a small difference in the pulse undershoot is observed (not shown here). The almost linear position dependence of the pulse height bodes well for the reconstruction of the particle position.

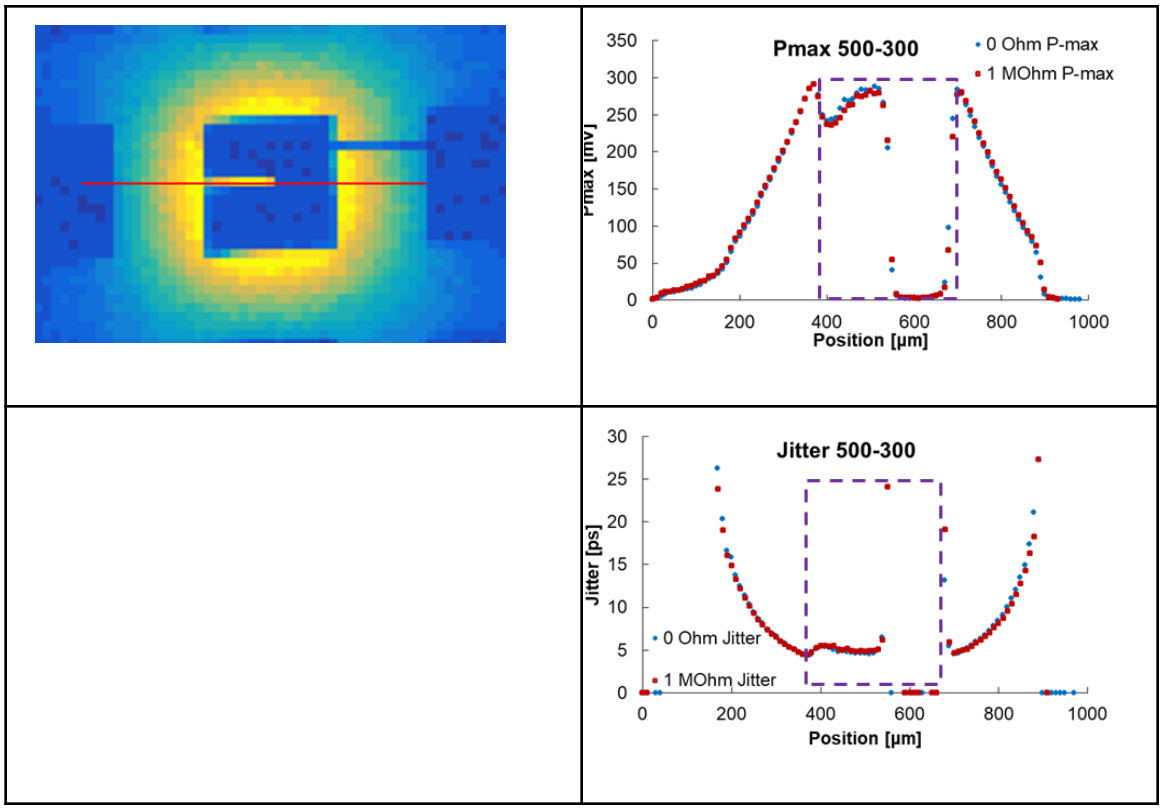

Figure 14: 2D distribution of the pulse height(left) and scans of pulse height (center) and jitter (right) for terminating the n++ layer by grounding it and via a 1 MΩ resistor to ground, respectively.

2. *Read-out electronics*

To address one of the questions by the committee on the precision of the accelerator clock, and its compatibility with the time resolution needed for the Roman Pots, we have initiated a discussion with accelerator experts. Their estimate of the EIC clock jitter RMS is 250 fs. Long term drift of the clock will need to be assessed, but can be compensated. More discussions with accelerator experts are needed, but this preliminary assessment of the accelerator clock is encouraging.

For the first time an AC-LGAD sensor was assembled with and read out by an ALTIROC chip, developed for the ATLAS timing detector (HGTD). This chip is designed in the CMOS TSMC 130 nm technology and uses TDCs to measure the Time of Arrival and Time over Threshold, as well as RAM for data buffering. The maximum jitter of the ALTIROC is in the order of 25 ps for 10 fC charge. For this test an early prototype ATIROC0 v1 was used and a strip AC-LGAD with pitch 100 um, and inter-strip gap of 20 um, operated at -250 V. The ALTIROC0 chip is a 4 channel prototype that implements an analog readout after the preamplifier, and a digital readout after the discriminator. The chip implements two types of preamplifiers (a voltage preamplifier and a trans-impedance preamplifier), and a classical threshold discriminator (a CFD was

implemented in following versions of the chip). The chip is wire-bonded to a dedicated PCB that mounts an FPGA for the signal handling and buffering. Figure 15 shows the signals generated by beta particles from a ^{90}Sr source, as read out by the analog and digital channels of the ALTIROC chip. While more studies are on-going, including with lasers, these preliminary results are very encouraging as they suggest a compatibility between AC-LGAD signals and ALTIROC input channels, and pave the way for the development of an ALTIROC chip which builds upon the design made for ATLAS and matches it to the specifications of the Roman Pots at EIC, e.g. 500 um pitch.
In parallel, a test bench has been set up at IJCLab in order to read the AC-LGAD produced by BNL with the ALTIROC1 chip, a newer prototype of the ALTIROC chip, with close to final analog and digital circuits. The AC-LGAD sensor is expected to be wire-bonded to the ALTIROC1 chip at BNL in the coming weeks, and the measurements at IJCLab will start in April.

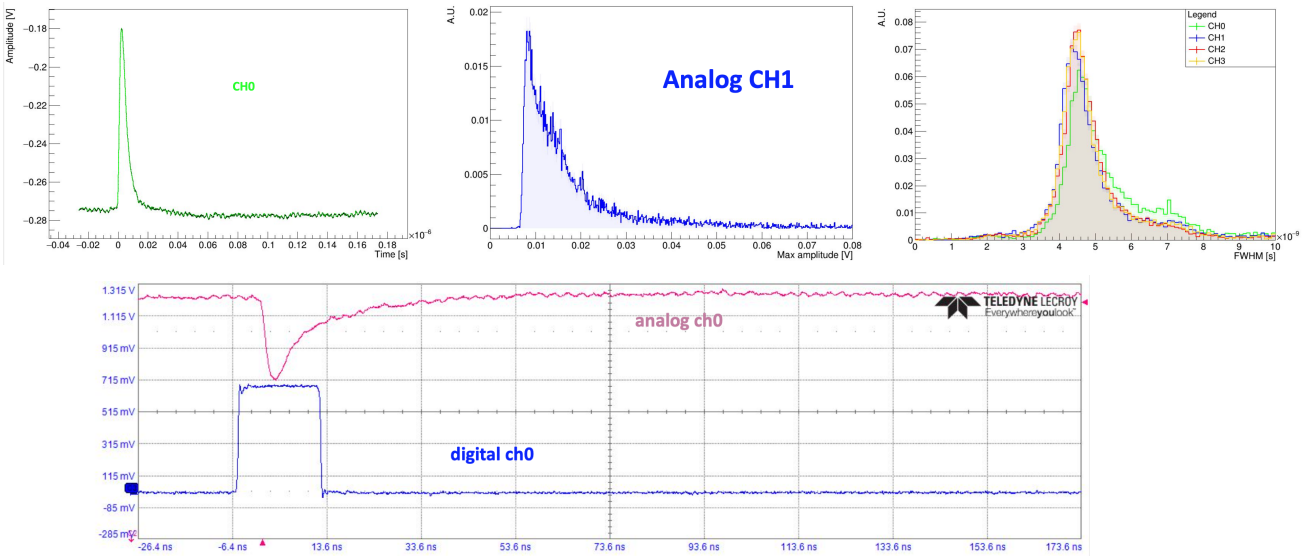

Figure 15: Signals read out by an ALTIROC0 v1 ASIC, assembled with an AC-LGAD strip sensor of 2x2 mm^2, with pitch 100 um, and inter-strip gap 20 um. An analog signal waveform in channel 0 (top-left), the amplitudes of the analog signals in channel 1 (top-middle), the FWHM of the analog signals in channels 0, 1, 2 and 3 (top-right), an analog and digital signals from channel 0 in the oscilloscope (bottom).

The work of redesign of the ALTIROC chip to meet the EIC requirements was started by the team at IJCLab and OMEGA. The first step consisted in coming up with a detailed list of specifications for EIC, paying particular attention to the ones significantly different from the ATLAS timing detector (HGTD). Extensive discussions have been ongoing between electronics experts at IJCLab/OMEGA, and sensors experts as well as EIC machine experts at BNL. While some parameters are still uncertain, we have identified the main modifications that will need to be made to the ALTIROC original design. The primary challenge consists of the smaller pixel size required for EIC Roman Pots. If using the same front end concept (preamplifier, discriminator and two TDC for Time of Arrival and Time Over Threshold), the needed surface is estimated to be < 150000 µm^2. As the

occupancy in the EiC Roman Pots is very small and the readout trigger-less, the remaining area in the pixel should be sufficient for the pixel digital part (ALTIROC is using a 35 µs depth SRAM that is not necessary for EIC applications). The option of using an ADC measurement instead of a TOT is currently considered, and the area needed for such an ADC would be compatible with the pixel area. Simulations are needed to evaluate the ADC characteristics (dynamics, linearity, power dissipation…).

With an ASIC of 32x32 channels, the ASIC is expected to have a larger power density of the ALTIROC ASIC. An estimate of the target ASIC power dissipation has been made based on the ALTIROC chip for the ATLAS timing detector. A per pixel power dissipation of 3 mW is estimated assuming, conservatively, a 10% occupancy, for a total of 3.072 W per chip, including the peripheral electronics. This corresponds to 1.067 W/cm^2 and a total power dissipation in the whole detector of 1.573kW (see Strawman layout). This estimate has to be compared to the corresponding power consumption for the ATLAS timing detector: 1.2 W/chip (300 mW/cm2) and a total power dissipation of 19.3kW. Taking into account the lower capacitance in AC-LGADs than in standard LGADs, as used in ATLAS, we might reduce the size of the transistor in the preamp and reduce its power dissipation. In addition, the 10% occupancy is a very conservative estimate (occupancy estimation in the Roman Pots is <<0.1%) and this will further reduce the ASIC power consumption.

The design of a 4x4 channels prototype will start at OMEGA in spring 2021 in CMOS TSMC 130 nm with an expected submission end 2021.

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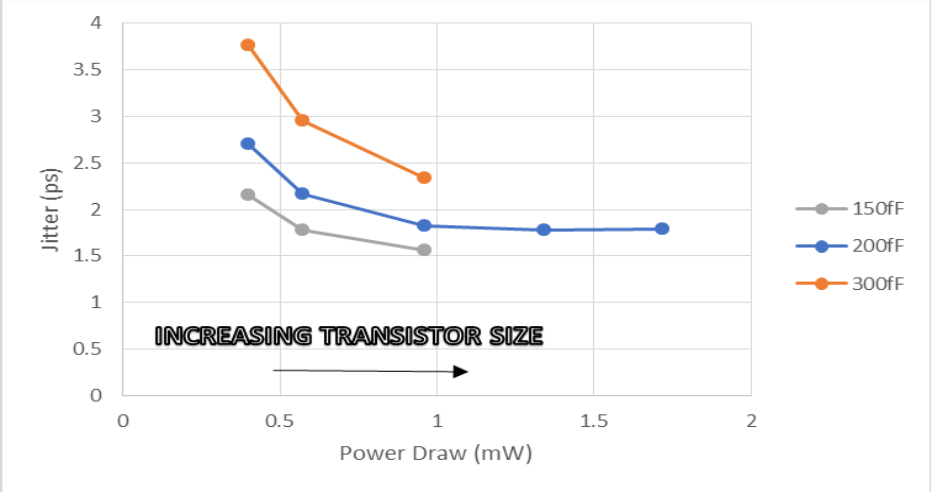

Guided by the measurements made on sensors the UCSC team has embarked on a program to develop an ASIC that would be matched to the pitch (~500 microns) and power (<500 µW) goals mentioned earlier. The technology chosen for the front-end is SiGe bipolar because of the potential for speed and low power. Other groups are

exploring various CMOS options so we can expect to have comparative information on technology choices in 2022. We are working on a design in collaboration with a small company, Anadyne, Inc. We have worked before with the technical personnel at the company and they have developed ASICs in SiGe for many years. To look at the most ambitious goal of 15 psec resolution, we have been simulating the signal expected for a 20 micron thick sensor. To achieve the timing goal we want the jitter contribution to be << 10 psec. Figure 5 shows a simulation based on a cadence design of a trans-impedance amplifier, which shows that the technology can meet our goals.

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In addition, based on the recommendations by the Committee, and given the similarity of the two proposals that are based on the same AC-LGAD sensor technology, we have established a close collaboration with the eRD29 *"Precision Timing Silicon Detectors for Particle Identification and Tracking at EIC"* team: F. Geurts (Rice), W. Li (Rice), S. Yang (Rice), C. Loizides (ORNL), C. Royon (Kansas).

In addition, we have also established a Consortium of 14 internationals institutes and 33 scientists with interests in the LGAD technology for EIC detectors. See Expression of Interest on "*Fast timing silicon detectors for EIC detectors*", https://indico.bnl.gov/event/8552/contributions/43183/attachments/31235/49294/EIC.EoI_LGAD_consortium.pdf. Two meetings have already taken place and future discussions on dedicated topics are planned in the coming weeks and months, see indico folder of the agendas https://indico.bnl.gov/category/323/

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The direct cost for the Roman Pots detector (excluding labor as well as R&D and pre-production cost) is estimated to be $1.2M, based on experience building the ATLAS timing detector. The following table shows the breakdown of the estimated costs. The total cost includes a 1.33 factor that accounts for an underestimation of the Strawman detector layout cost, based on the experience of cost underestimation for the ATLAS timing detector in the LOI with respect to the TDR.

Item	Cost [k$]
Sensors	260
ASICs	280
Peripheral Electronic Boards (lpGBT, VTRX, DC-DC conv., PCB, connectors)	25
LV and HV systems	45
Cables (LV,HV,DCS), Electrical connectors	70
Fibers, Optical connectors	20
Module Assembly (incl. hybridisation, flexes, assembly)	90
Cooling system	70
Mechanics (on-det cooling plate, suport plate cooling, hermetic vessel)	30
TOT	**890**
TOT*1.33	**1,200**

What was not achieved, why not, and what will be done to correct?

The design of a double-metal for the definition of complex 2D metal patterns is waiting for results from the test-beams. It takes little time to design and fabricate the photolithographic mask itself, so it is not urgent to have it in house right now. As soon as results are available and well understood, it will be clear which designs are worth pursuing. The mask will be designed and implemented in a couple of wafers that are awaiting this last process step.

How did the COVID-19 pandemic and related closing of labs and facilities affect progress of your project?

The pandemic has affected the presence of technicians, postdocs and scientists at BNL, and delayed considerably the assembly and bonding of sensors, and in turn the pace of sensor testing.

How much of your FY20 funding could not be spent due to pandemic related closing of facilities?

The FY20 funds were all spent for the fabrication of the sensors, despite the reduced presence of person-power in the labs due to the pandemic.

Do you have running costs that are needed even if R&D efforts have paused?

No

Future

What is planned for the next funding cycle and beyond? How, if at all, is this planning different from the original plan?

The work planned for the next period is structured in three main tiers:

1) Performance studies
    a) Implement an updated layout of sensors in the Roman Pots detector subsystem - based on the options laid out in the straw-man in the present document - to assess the impact of the more realistic experimental setup at the EIC.
    b) Build on Yellow Report studies using detectors outside the beam pipe for protons from nuclear breakup (e.g. e+d -> p' + n' + e'; so-called "off-momentum" detectors). The same AC-LGAD technology could be employed for this subsystem, and similar detailed studies of acceptance, backgrounds, etc. could be completed to assess the usefulness of the AC-LGAD technology for this physics application.

2) Sensor development
    a) Analyse data from the two recent test-beams,
    b) Continue testing of existing AC-LGAD to establish optimized fabrication parameters, for example perform TCT laser scans to study signal sharing properties and compare results with test-beam measurements,
    c) Fabrication of sensors with varied doping of the resistive n-type layer to assess its impact on signal sharing,
    d) Compare TCAD simulations with experimental results from lab and test-beam measurements,
    e) Fabrication and testing of a large area prototype with design and layout towards the Roman Pots specifications: 500 μm pitch pixels, 1.4 x 1.4 cm^2,
    f) Produce thin AC-LGAD (~20 μm) to improve time resolution.

3) ASIC development
    a) Continue testing of ALTIRC0 + AC-LGAD, for instance with IR lasers and possibly at test-beams (if beam-time schedule allows) to assess

collection properties in greater detail, signal sharing between channels, dependence of time-over-threshold (TOT) on input signal charge.

b) Assemble a newer ALTIROC prototype, ALTIROC1 + AC-LGAD and study the CFD implementation in the new chip.
c) Intensify the discussion with EIC accelerator experts on clock jitter, transmission etc.
d) Characterize ALTIROC1 + AC-LGAD using a similar test bench as the one used by ATLAS/HGTD.
e) Complete the redesign of the ALTIROC chip to meet the specifications of the Roman Pots of EIC. The chip production is expected in the beginning of calendar year 2022.
f) Study alternative, low-power ASIC technologies, and perform market survey of SiGe technology. Radiation testing of SiGe technologies.

What are critical issues?

The main single critical issue is the reopening of the laboratories in BNL's Instrumentation Division and ramping up with the testing of the devices.

In so far as sensor R&D, the main technical critical issue is the convergence of the preliminary studies of different electrode shapes and slim edges such that we can start the production of a relatively large-scale prototype that includes those features and can be tested in the lab and in test-beams.

Additional information:

We will continue reaching out to the wide community of scientists interested in application of LGADs at EIC to share expertise and solutions to common challenges. In this perspective we will continue the so-far successful discussions in the LGAD Consortium that was initiated a few months ago for the submission of LOIs, as mentioned above.

Manpower

The manpower for the new period is the same as the one committed in the previous period, and includes contributed labor for simulations to determine scientific requirements, for the sensor development and testing, as well as for studies on electronics:

- Funded by EIC R&D:
    - Wei Chen, BNL engineer, Instrum. Div. (10%).
- Not funded by EIC R&D
    - A. Tricoli, physicist (10%), G. Giacomini, scientist (10%), G. D'Amen,

postdoc (30%), Enrico Rossi, professional (10%) at BNL.
    - 0.15 FTE E.C. Aschenauer to supervise the simulations to determine the scientific requirements.
    - 0.4 FTE of a PostDoc in the group of E.C. Aschenauer to perform the needed simulations.
    - 0.25 FTE of a PhD student (W. Chang) in the group of E.C. Aschenauer to perform the needed simulations.
    - 0.10 FTE of C. Da Via at SBU/Manchester to supervise a student on sensor testing.
    - 0.10 FTE of M. Benoit (BNL Physics Dept.) for electronic readout developments and simulations.
    - 0.6 FTE, (50% engineers at OMEGA, 50% physicist at IJCLab involved in ATLAS and EIC studies) for ASIC design.
    - 0.20 FTE from the UCSC team.
    - IJCLab-Orsay: D. Marchand, physicist (40%), C. Munoz, physicist (30%), L. Serin, physicist (20%), P.K. Wang, grad student (50%).
    - OMEGA: C. de la Taille, engineer (20%), M Morenas, grad student (30%).

External Funding

- For the simulation part of the proposal we utilize funds from the approved 3-year program development project "*eRHIC: from Virtual to Real*" of E.C. Aschenauer to support the labor needed to perform all the simulations.
- For the silicon R&D part of this project we will leverage resources from A. Tricoli's Early Career Award and LDRD for the development of fast-timing silicon detectors (LGADs) for HEP and photon science, respectively.
- Award in 2020: A.Tricoli as co-investigator in the project for the US-Japan Science Cooperation Program for HEP, titled *"Development of precision timing silicon detectors for future high energy collider experiments [renewal]"*, $37,000 awarded to BNL in FY21.
- Award in 2021-2022 to IJCLab/OMEGA in order to produce a prototype of ASIC to readout an AC-LGAD meeting the requirements of the Roman Pots of EIC. Award by French P2IO consortium in the amount of $90,000.

Publications

- A. Apresyan, G. Giacomini, A. Tricoli et al., "Measurements of an AC-LGAD strip sensor with a 120 GeV proton beam", JINST 15 P09038 (2020).